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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,791	03/31/2001	Manoj Khare	42390P9872	7416

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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,791	KHARE ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,11-16 and 18-23* is/are rejected.

7)☒ Claim(s) *6,10,17,24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Application No. 10/128,962 filed March 31, 2001. Claims 1-24 are pending in this application.

2. The specification and the claims have been examined with the results that follow.

Claim Objections

3. Claim 20 is objected to because of the following informalities:

In claim 20, line 2, before "the outgoing", delete –the--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5, 7, 15-16, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Audityan et al (US6,256,713).

As per claim 1, Audityan discloses a method comprising: receiving a read request relating to a first line of data in a coherent memory system [*a collision is determined by comparing the address received for the read*; col. 3, lines 20-25]; receiving a write request

relating to the first line of data at about the same time as the read request is received [*a collision is determined by comparing the address received for the write*; col. 3, lines 20-25]; detecting that the read request and the write request both relate to the first line [*if the address match, then a collision occurs*; col. 3, lines 24-32]; determining which request of the read and write request should proceed first [*if there is collision, read has priority*; col. 3, lines 52-58]; and completing the request of the read and write request which should proceed first [*reads are processed before any writes*; col. 3, lines 50-55].

As per claim 2, Audityan discloses the read request is received first, the read request is determined to be the request which should proceed first [*read transaction(s) in the read queue are processed according to entries in order buffer 206*; col. 3, lines 39-44, 55-58].

As per claim 3, Audityan discloses the write request is received first, the write request is determined to be the request which should proceed first [*write transaction(s) in the write queue are processed according to entries in order buffer 206*; col. 3, lines 39-44, 55-58].

As per claim 4, Audityan discloses delaying the request which is not the request which should proceed first [*if no collision is pending, read transactions are processed before any writes*; col. 6, lines 59-61].

As per claim 5, Audityan discloses the read request is received first, the read request is determined to be the request which should proceed first, the write request is delayed [col. 1, lines 30-32].

As per claim 7, Audityan discloses detecting that the read request and the write request both relate to the first line is accomplished by comparing an address of the read request and an address of the write request [*address matching*; col. 3, lines 24-32].

As per claim 23, Audityan discloses completing the request of the read and write request which was not determined to be the request which should proceed first [col. 5, line 62 – col. 6, line 1].

As per claim 15, Audityan discloses an apparatus comprising: means for receiving a read request relating to a first line of data in a coherent memory system [*a collision is determined by comparing the address received for the read in read queue 202*; col. 3, lines 13-25]; means for receiving a write request relating to the first line of data at about the same time as the read request is received, the means for receiving a write request coupled to the means for receiving the read request [*a collision is determined by comparing the address received for the write queue 204*; col. 3, lines 20-25]; means for detecting that the read request and the write request both relate to the first line, the means for detecting coupled to the means for receiving the write request and the means for receiving the read request [*queue logic 200 coupled to read queue 202 and write queue 204 determines if there is an address match, then a collision occurs*; col. 3, lines 24-32]; means for determining which request of the read and write request should proceed first, the means for determining coupled to the means for detecting [*arbitration logic 216 determines if there is collision, read has priority*; col. 3, lines 52-58]; first means for completing the request of the read and write request which should proceed first, the first means coupled to the means for

determining, the means for receiving the read request and the means for receiving the write request [*read queue bus 226 coupled to read queue 202 and write queue 204*; Fig. 2]; and second means for completing the request of the read and write request which was not determined to be the request which should proceed first, the second means coupled to the means for determining, the means for receiving the read request and the means for receiving the write request [write queue bus 228 *coupled to read queue 202 and write queue 204*; Fig. 2].

As per claim 16, Audityan discloses means for delaying the request which is not the request which should proceed first, the means for delaying coupled to the means for determining and to the first means and the second means [*if no collision is pending, read transactions are processed before any writes; queuing logic 200 coupled to read queue 202 and write queue 204*; col. 6, lines 59-61].

6. Claims 11-14, 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by VanDoren et al (US6,122,714).

As per claims 11 and 18, VanDoren discloses a system comprising: a first processor [*processor 12a*; Fig. 3]; a second processor [*processor 12b*; Fig. 3]; a scalability port coupled through a bus to the first processor and coupled through the bus to the second processor [*global port coupled to each processor through lines coupled to each SIB*; Fig. 3],

the scalability port including: an incoming request buffer to store requests relating to read and write operations, the requests including addresses to be read or written [col. 19, lines 49-53]; an outgoing request buffer to store requests relating to read and write operations, the requests including addresses to be read or written, coupled to the incoming request buffer [col. 27, lines 49-57]; bus logic to interface with the bus, the bus logic coupled to the incoming request buffer and the outgoing request buffer [*switch coupled to input and output buffers*; Fig. 25]; a snoop pending table to contain entries related to cache lines coupled to the incoming request buffer and the outgoing request buffer [*TTT enforce an order of requests that are issued or received*; col. 3, lines 8-12]; a snoop filter coupled to the snoop pending table [*requests are either ignored or delayed*; col. 3, lines 25-30]; and control logic to interface with and coupled to the incoming request buffer, the outgoing request buffer, and the bus logic, the control logic to compare addresses of requests of the incoming request buffer and outgoing request buffer and detect identical addresses among requests of the incoming request buffer and the outgoing request buffer [*each processor includes logic to detect an outstanding read to the same cache location*; col. 51, lines 57-65], the control logic to stall a second request of the incoming request buffer and the outgoing request buffer pending completion of a first request of the incoming request buffer and the outgoing request buffer when the second request and the first request include identical addresses [*probes are stalled if there is a read to the same location*; col. 51, lines 57-65].

As per claims 14 and 19, VanDoren discloses a memory coupled to the scalability port [*memory 13*; Figs. 3, 6]; and wherein the scalability port further includes: a

memory controller to interface with and control the memory, the memory controller coupled to the incoming request buffer, the outgoing request buffer, the bus logic, and the control logic [*main arbiter 27 coupled to the global port, to memory 13 and processors 12*; Fig. 3]; and wherein: the control logic to pass requests to the memory controller to read from or write data to the memory [*arbiter 27 manages data movement between the resources and the switch*; Fig. 3; col. 8, lines 10-23].

As per claims 12 and 20, VanDoren discloses the outgoing request buffer and incoming request buffer to receive read requests and write requests from the bus through the bus logic, the read requests and write requests each individually originating from one of the first processor or the second processor [col. 27, lines 49-57; col. 6, lines 50-59].

As per claims 13 and 21, VanDoren discloses the control logic to pass requests to the outgoing request buffer and to the incoming request buffer to write data to or read data from a cache associated with the first processor [col. 27, lines 49-57].

As per claim 22, VanDoren discloses the control logic further to pass requests to the outgoing request buffer and to the incoming request buffer to write data to or read data from a cache associated with the second processor [col. 27, lines 49-57].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Audityan et al (US6,256,713) and Bauman et al (US5,875,472).

As per claim 8, Audityan discloses the claimed invention as detailed above in the previous paragraphs. However, Audityan does not specifically teach the read request originates from a first processor and the write request originating from a second processor as recited in the claim.

Bauman discloses a first processor receiving a write request and a second processor receiving a read request in a multiprocessor system for performing address conflict detection (col. 1, lines 8-13, 49-62). Since the technology for implementing a first processor originating a write request and a second processor originating a read request was well known and since a first processor originating a write request and a second processor originating a read request improves the system by performing address conflict detection, an artisan would have been motivated to implement a first processor originating a write request and a second processor originating a read request in the system of Audityan. Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Audityan to include a first processor originating a write request and a second processor originating a read

request because it was well known to improve the system by performing address conflict detection as taught by Bauman.

As per claim 9, Audityan discloses the read request is received first, the read request is determined to be the request which should proceed first, the write request is delayed [col. 1, lines 30-32].

Allowable Subject Matter

9. Claims 6, 10, 17 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

As per claims 6, 10 and 17, the prior art of record does not teach or suggest "the read request is delayed and further comprising: satisfying the read request with a new value, the new value coming from the write request" in combination with the other elements set forth in the claimed invention.

As per claim 24, the prior art of record does not teach or suggest "completing the request includes the read request completing the write request independent of an origination node of the write request" in combination with the other elements set forth in the claimed invention.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach buffering read and write request, resolving conflict between concurrent read and write requests.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 28, 2004

Pierre M. Vital
Examiner
Art Unit 2188